A New Generation of Microwave Sweepers

The HP 83750 family of microwave sweepers achieves a new level of swept frequency accuracy by being fully synthesized in all sweep modes, including fast analog sweeps. It also uses fundamental oscillators for improved signal purity.

by Alan R. Bloom, Jason A. Chodora, and James R. Zellers

Swept-frequency microwave signal sources (sweepers), have long been considered basic equipment for component test applications. Sweeper capabilities also satisfy many general-purpose needs, both in the laboratory and in production.

The first HP microwave sweeper, the HP 670A, employed a klystron oscillator, which was mechanically swept by means of a motor drive. Sweep speed capability was improved considerably in the 1960s by the HP 8690 Series, which employed an electronically-tuned backward-wave oscillator (BWO). In the 1970s, the HP 8620 Series achieved new levels of reliability by replacing BWO tubes with solid-state YIG oscillators. In 1980, microprocessor control was added in the HP 8350 Series sweepers[1] to provide full programmability and many convenient user features.

The frequency accuracy of most sweepers, including those mentioned above, is limited by the microwave oscillator and its drive electronics. Newer synthesized sweepers, such as the HP 8360 Series,[2] achieve excellent frequency accuracy in CW and stepped-sweep modes. In continuous-sweep mode, however, they provide synthesizer correction only at the beginning and the end of each sweep band—there is no frequency correction during the actual sweep. The HP 83750 Series (Fig. 1) establishes a new standard of swept frequency accuracy by being fully synthesized in all sweep modes, including fast analog sweeps.

The HP 83750 Series of synthesized sweepers is part of the HP 8370 family of microwave sources. This family also includes CW generators and synthesized signal generators, which are discussed in the article on page 6. Four HP 83750 sweeper models are currently available:

- HP 83751A: 2 to 20 GHz, +10 dBm
- HP 83751B: 2 to 20 GHz, +17 dBm
- HP 83752A: 0.01 to 20 GHz, +10 dBm
- HP 83752B: 0.01 to 20 GHz, +16 dBm from 0.01 to 2 GHz, +17 dBm from 2 to 20 GHz.

Extended frequency coverage to 110 GHz is available with HP 83550 Series millimeter heads, using the optional source module interface. Other options include a 70-dB attenuator, a high-stability time base, and alternate output connector type and location. For field test applications, a portable package is also available, which adds a tilt-bail handle, rubber bumpers, rear feet, and a protective front-panel cover.

Fundamental Oscillator Technology

The RF block diagram of the HP 83752A sweeper appears in Fig. 2. A dual YIG oscillator (DYO) generates a microwave signal between 2 and 20 GHz using two separate oscillators mounted in a common magnet assembly (see article, page 46). One oscillator tunes from 2 to 11 GHz, and the other tunes from 11 to 20 GHz.

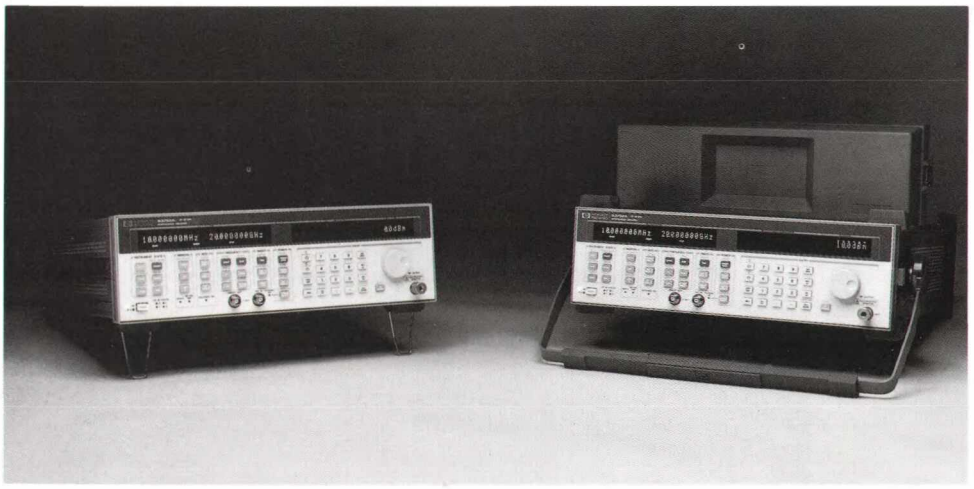


Fig. 1. The HP 83750 Series synthesized sweepers are packaged in a standard five-inch-high cabinet. They fit in the same rack panel space as the older HP 8350 Series nonsynthesized sweepers.

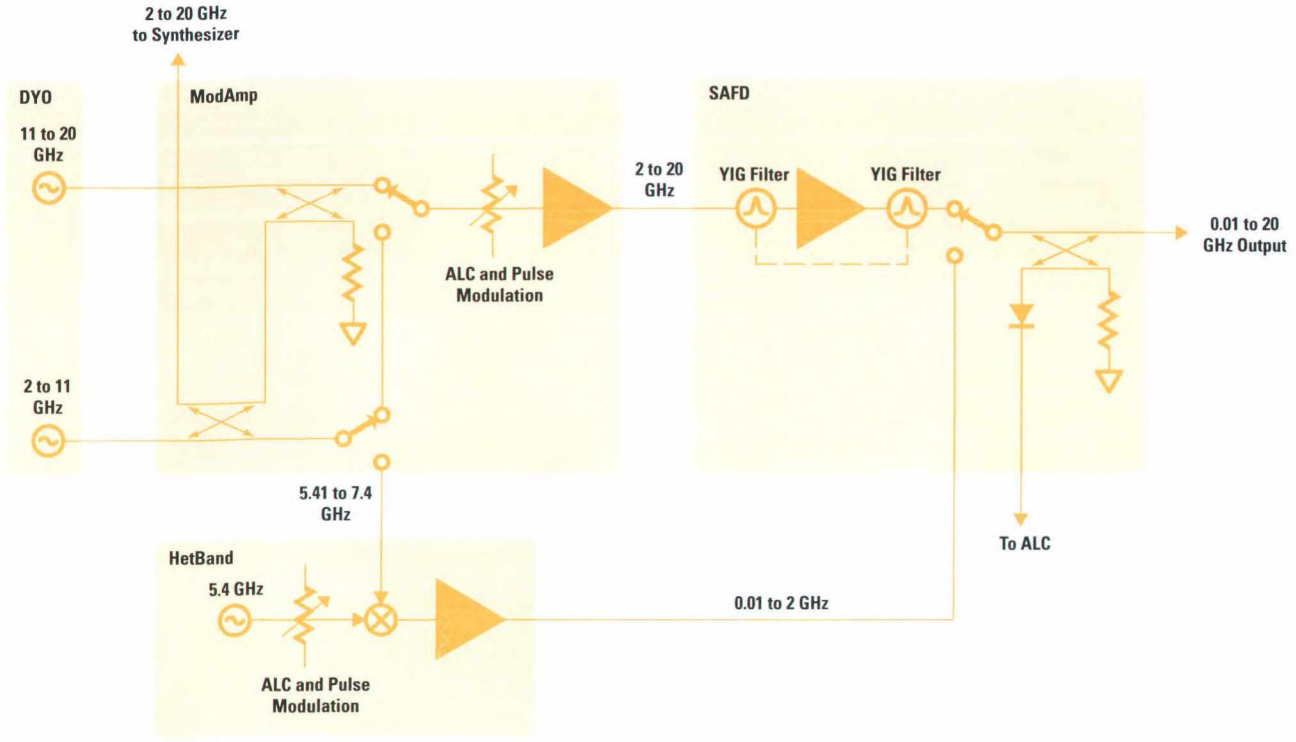


Fig. 2. RF block diagram of the HP 83750 Series sweepers. The RF chain includes four new microcircuit designs.

Previous HP sweepers used a lower-frequency oscillator multiplied up to the desired output frequency. The advantage of the fundamental oscillators in the HP 83750 is that they produce no subharmonics.

The two oscillator outputs feed into a modulator amplifier (ModAmp) microcircuit, which provides signal switching and distribution, amplification, and ALC and pulse modulation (see article, page 46). A low-level output goes to the sampler assembly for use by the synthesizer.

The main 2-to-20-GHz output signal from the ModAmp is routed to a switched amplifier filter detector (SAFD) microcircuit, which provides power amplification and two stages of YIG filtering (see article, page 46). The filtering reduces output harmonics to less than –45 dBc. A significant advantage of the YIG-filtered output is extremely low broadband noise, which is important for scalar network analysis applications.

The SAFD microcircuit also contains a broadband automatic level control (ALC) detector, which is used for power leveling over the entire 0.01-to-20-GHz frequency range. This technique avoids the power discontinuity commonly associated with sweepers that use separate leveling detectors for different frequency ranges.

To generate a signal below 2 GHz, the YIG oscillator is tuned between 5.41 and 7.4 GHz. This signal mixes with the output of a fixed 5.4-GHz synthesized oscillator to produce the 0.01-to-2-GHz output. An amplifier and filter follow. A major objective of this design was to reduce nonharmonic mixing spurious signals to less than –50 dBc for output levels less than +5 dBm, while minimizing broadband noise.

Frequency Control

The microwave oscillator and filter in the HP 83750 each contain a tiny sphere of crystalline yttrium iron garnet (YIG). When subjected to a magnetic field, a YIG sphere resonates at a microwave frequency that is directly proportional to the strength of the magnetic field. The sphere is mounted in the pole gap of an electromagnet. The field strength, and thus the YIG resonant frequency, are directly proportional to magnet current.

The job of the YIG driver, Fig. 3, is to generate a current proportional to the desired frequency. A sawtooth-shaped signal produced by the sweep generator board is scaled and offset by the YIG driver to sweep the YIG oscillator and filter over the desired frequency range. Smaller correction signals from the sweep generator compensate for nonlinearities and delays in the YIG frequency-versus-current response.

Even if the phase-locked loop synthesizer were not present, this architecture would produce a swept microwave signal with fair frequency accuracy. The synthesizer need only apply a small correction voltage to eliminate any remaining errors.

The function of the sweep generator board (Fig. 4) is to generate the main sweep ramp and several correction signals. Previous instruments used an integrator to form the sweep ramp. Such an integrator must be carefully designed to prevent its drift and nonlinearity from contributing to swept frequency error. In the HP 83750, a digital-to-analog converter (DAC) generates a stepped sweep ramp simultaneously with the analog ramp. Once per step, the two ramps are compared, and the sampled error voltage feeds back to correct

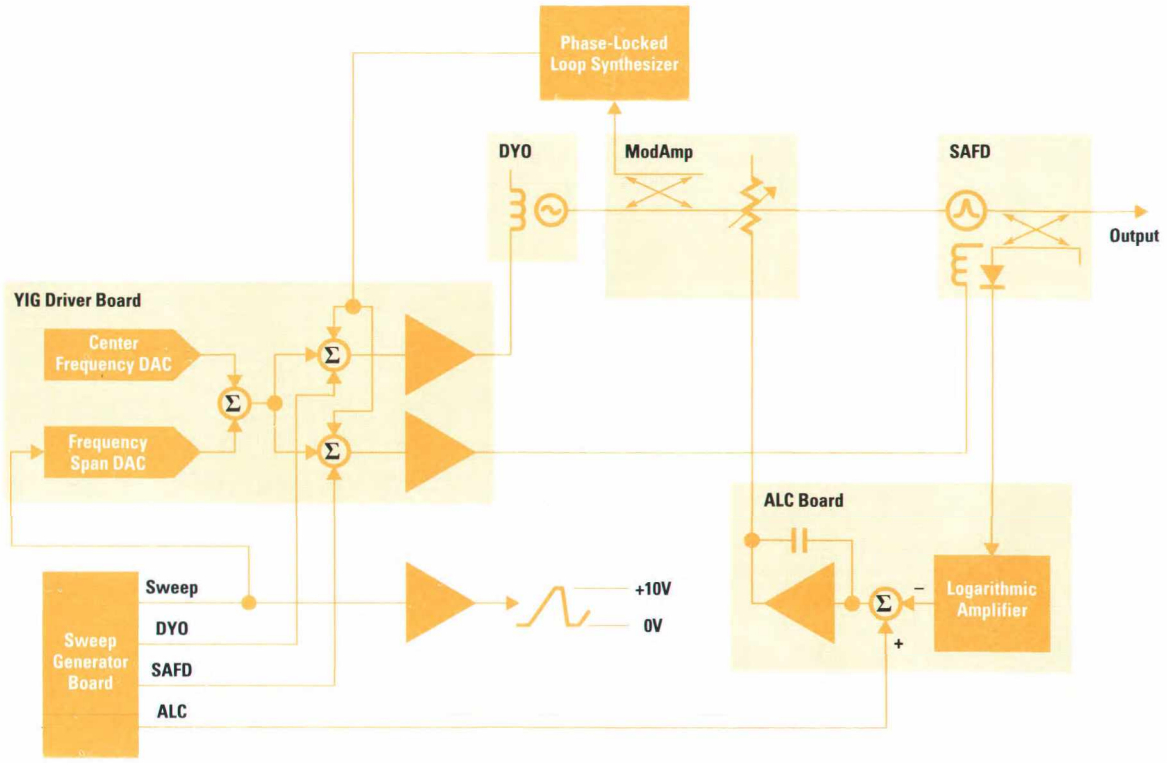


Fig. 3. HP 83750 frequency control block diagram. Unlike previous designs, the synthesizer in the HP 83750 remains locked throughout the sweep.

any integrator errors. The resulting sweep ramp reflects the accuracy and stability of the DAC output while retaining true analog sweep.

The analog sweep ramp is available to the user as a 0-to-10V ramp (**Sweep Out**) whose amplitude is independent of frequency span. Another output voltage (**V/GHz**) proportional to absolute frequency is also available. At the user's option, it can be scaled and offset to sweep between any two voltages between –10 and +10 volts.

The Digital Signal Processor

The digital sweep ramp and four correction voltages are generated by five DACs. A TMS 320C10 digital signal processor (DSP) calculates appropriate values in real time and loads

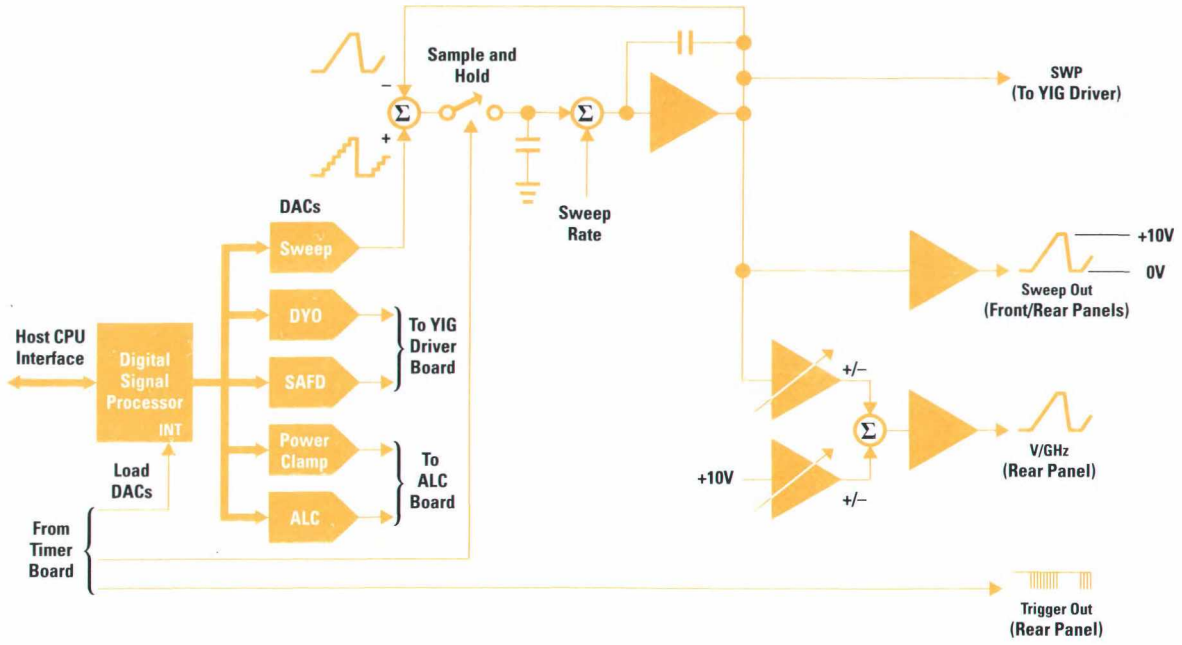


Fig. 4. The sweep generator assembly produces an analog ramp and four correction signals for use by other assemblies.

them into the DACs as the instrument sweeps. When the instrument is turned on, the host microprocessor (an MC68000) downloads calibration data to the DSP. After that, the host need only update the DSP with new start and stop frequencies, power, and sweep time whenever the user changes those values. The DSP automatically calculates the correction voltages based on that data.

The DACs are updated between 101 and 1601 times per sweep, depending on sweep time. A circuit on the timer board generates 101 to 1601 trigger pulses per sweep that are applied to the DSP interrupt input. The interrupt causes the DSP to update all five DAC outputs simultaneously.

The DSP has a minimum of about 100 microseconds between pulses to calculate upcoming DAC values. In this time, it must compute three third-order interpolations, one straight-line interpolation, two sweep ramps, and two complex delay compensation waveforms. A special third-order curve-fit algorithm is the key to achieving this performance using inexpensive DSP hardware (see below).

Two of the third-order interpolations are used to calculate linearity corrections for the DYO and SAFD. Actually, the synthesizer alone could correct for YIG oscillator nonlinearity, but there is no guarantee that the oscillator and filter are identical in this respect. The DSP correction ensures that the oscillator and filter track each other throughout the sweep.

Even more critical, for both tracking and swept frequency accuracy, is delay compensation. Whenever the current through a YIG magnet is changing, the YIG resonant frequency lags the current. The time lag is a function of sweep speed, start frequency, and previous history of magnet current. This delay causes fast transients to occur at the start of each band that are difficult for the synthesizer circuitry to correct for. The DSP uses a proprietary algorithm to calculate delay compensation, which is added to linearity correction and output to the appropriate DAC. Using the DSP to perform this function replaced a boardful of sensitive analog circuitry. It also made it easy to try many different compensation waveforms in our quest to achieve a new standard of swept frequency accuracy.

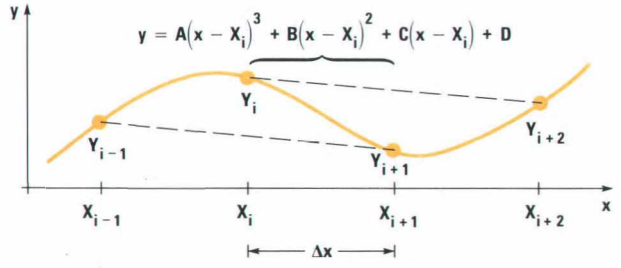
The third use of the third-order interpolation algorithm is for the power clamp output. The ALC board uses this signal to limit maximum RF drive level to the SAFD. Overdriving the YIG filter can cause squegging (low-frequency amplitude oscillations), which lowers the available output power.

The ALC output controls the instrument RF power level. The ALC board compares this signal to a logged version of the

Third-Order Curve-Fit Algorithm

The frequency-versus-current transfer function of a YIG oscillator or filter is only approximately linear. Production testing measures the deviation from linearity at a series of calibration frequencies and stores this information in the instrument's nonvolatile memory.

In Fig. 1, the Ys indicate the required correction at each calibration point. The Xs indicate the nominal frequency of each point. To interpolate between calibration points, we use a third-order curve y(x), defined by four parameters A, B, C, and D. A different set of parameters must be calculated for the interval between each pair of calibration points.



$$y(X_i) = Y_i \qquad D = Y_i$$

$$y(X_{i+1}) = Y_{i+1} \qquad C = (Y_{i+1} - Y_{i-1})/2$$

$$\frac{d}{dx}y(X_i) = \frac{Y_{i+1} - Y_{i-1}}{2\,(\Delta x)} \qquad A = C + 2D + (Y_{i+2} - Y_i)/2 - 2(Y_{i+1})$$

$$\frac{d}{dx}y(X_{i+1}) = \frac{Y_{i+2} - Y_i}{2\,(\Delta x)} \qquad B = -A - C - D + Y_{i+1}$$

(Δx normalized to unity)

Fig. 1. This third-order algorithm produces an interpolated curve that passes exactly through each calibration point and has a continuous first derivative. Only add and shift operations are required to compute the coefficients A, B, C, and D.

The most straightforward way to calculate the four parameters is to generate four equations by setting y(x) equal to the four closest calibration points, and then solve for the four unknowns A, B, C, and D. Besides being computationally intensive, this method results in sharp edges at calibration points, that is, it has a noncontinuous first derivative.

A well-known method called the cubic spline uses all N available calibration points to generate a curve with continuous Nth-order derivatives. Unfortunately, the calculations would take much longer than the available 100 μs. Other interpolation algorithms, such as the B spline, are faster, but the resulting curve does not pass exactly through the calibration points.

The method employed in the HP 83750 Series sweepers uses four equations to solve for the four unknowns. Two equations result from constraining the curve to pass exactly through the two nearest calibration points, Y_i and Y_{i+1}. The other two equations result from setting the slope of the curve at the segment endpoints equal to the slope of a line connecting the two points that bracket each endpoint. This guarantees that the slope of each segment will match the slope of the adjacent segment where the segments connect, so there will be no sharp edges.

Solving these four equations results in the equations for A, B, C, and D shown in Fig. 1. Note that all multiplications and divisions are by factors of two. This makes the computation very efficient since multiplying or dividing by 2 is equivalent to shifting the binary number left or right one bit. Shifting can occur automatically as the DSP loads the number into its accumulator.

Calculating A, B, C, and D requires 33 DSP cycles or 6.6 μs. The total time to do all computations required for the three separate interpolated outputs is 153 cycles or 30.6 μs.

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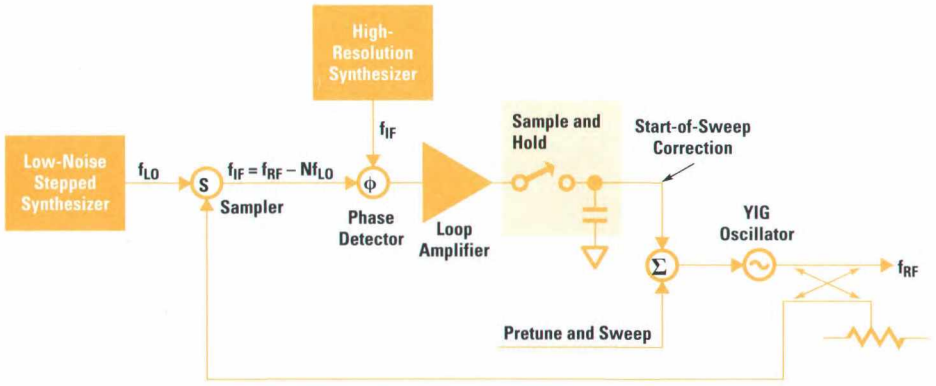

Fig. 5. Traditional synthesizer block diagram. In the traditional "lock and roll" synthesizer, the YIG oscillator is phase locked at the start of the sweep to a multiple of a low-noise, stepped CW synthesizer frequency. The analog correction voltage from the phase detector is sampled and held for the duration of the sweep.

detected RF output level and adjusts modulator current to make the two signals equal. Detector calibration and temperature compensation are handled by additional circuitry on the ALC board. The DSP ALC signal includes basic RF power level, flatness compensation, and power sweep.

"Flatness compensation" refers to the use of factory calibration arrays to correct for the frequency response of the coupler detector located in the SAFD. In addition, the user can enter arrays of up to 801 points to correct for the response of the user's test system. These user calibration points can be at any frequencies within the instrument's range. Since the third-order algorithm requires equally spaced calibration points, ALC flatness compensation must use linear interpolation.

Synthesizer

Hewlett-Packard microwave synthesizers (for example the HP 8360 Series) have traditionally used the block diagram shown in Fig. 5. The local oscillator (LO) drive for the sampler is a low-noise stepped synthesizer. Its output has coarse frequency resolution, but extremely low phase noise. It is not able to sweep its output frequency. The IF output of the sampler is then locked to a high-resolution synthesizer, often a fractional-N loop, which provides the output frequency resolution.

The only loop in the traditional block diagram with swept capability is the fractional-N loop. It is used as the reference for the sampler IF phase-locked loop. Therefore, its output is directly translated (mixed) to the RF output. This limits the width of a synthesized sweep to the width of a fractional-N sweep, which is typically tens of megahertz. For broader sweeps, the traditional synthesizer must sweep unlocked. The start frequency is phase locked, then the phase-locked loop error voltage is sampled and held while the frequency sweeps open-loop. This technique is called "lock and roll." Later instruments use the synthesizer to count the stop frequency and apply a correction to subsequent sweeps. This makes both the start and stop frequencies quite accurate, but the actual sweep is still performed open-loop with significant frequency errors between the endpoints.

In the HP 83750 (Fig. 6), the fractional-N loop is used as the LO for the sampler. The fractional-N loop output frequency is multiplied by the harmonic number and translated to the RF output. This gives the HP 83750 the ability to perform true synthesized broadband analog sweeps. If the fractional-N loop sweeps an octave, the RF output will sweep an octave. For example, the HP 83750 can sweep the full 11-to-20-GHz RF band in one continuous phase-locked sweep. This improves the swept frequency accuracy of the instrument by at least an order of magnitude (Fig. 7). Swept frequency errors are now limited to timing uncertainties and transients that cannot be completely removed because of limited phase-locked loop bandwidth. Both of these errors improve linearly with reduced sweep speed and span. This architecture gives the HP 83750 Series state-of-the-art swept frequency accuracy, allowing very precise, high-speed swept measurements.

The HP 83750 fractional-N assembly contains a voltage-controlled oscillator (VCO), a fractional divider, and a phase-locked loop. This circuitry can synthesize a 250-to-500-MHz signal with resolution better than 10 nHz and excellent swept frequency accuracy and phase noise (see page 44). The fractional-N phase-locked loop output is the LO drive for the microwave sampler. A coupler sends a portion of the YIG oscillator output signal to the RF port of the sampler. The action of the sampler in the frequency domain is similar to that of a harmonic mixer. The IF output frequency f_{IF} of the sampler is a function of the LO and RF frequencies f_{LO} and f_{RF} and the harmonic number N:

$$f_{IF} = f_{RF} - Nf_{LO}.$$

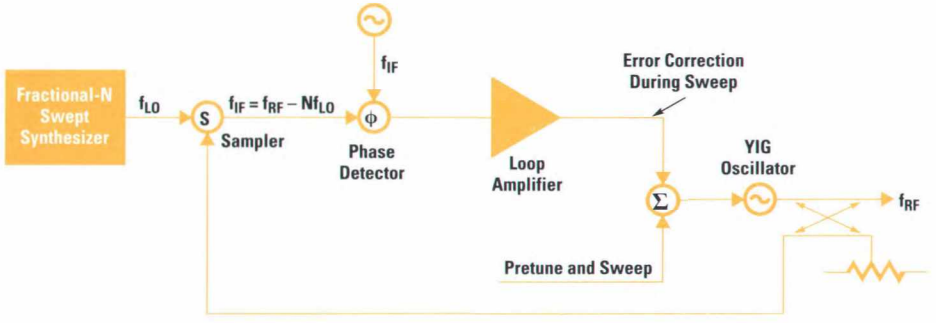

Fig. 6. HP 83750 synthesizer block diagram. In the HP 83750 synthesizer, the YIG oscillator is phase locked to a multiple of a fractional-N synthesizer frequency during the sweep.

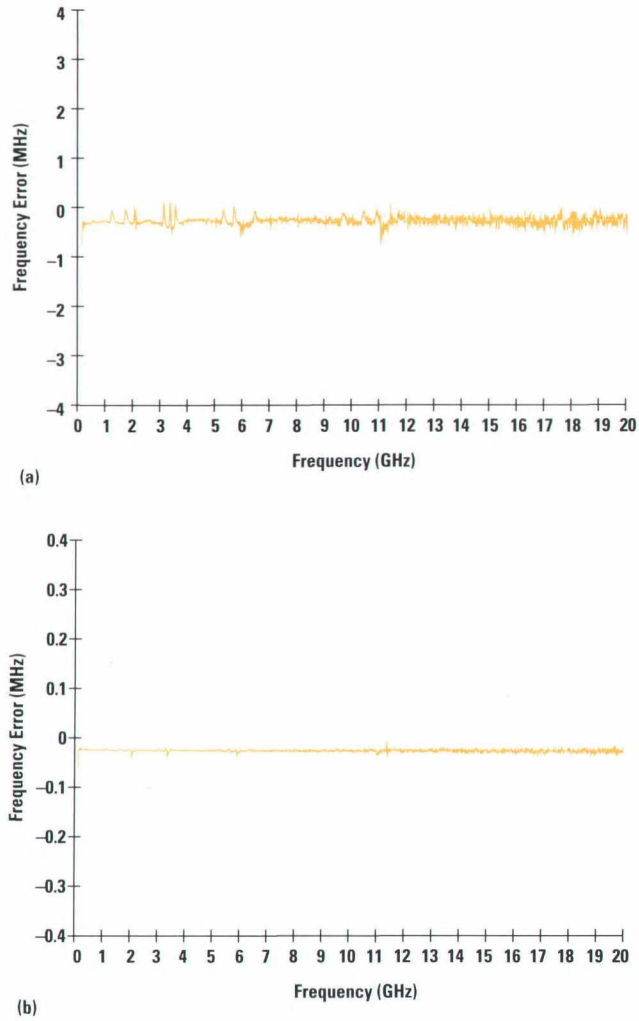

Fig. 7. (a) HP 83750 swept frequency accuracy with a 100-ms sweep. (b) Improvement obtained at a slower sweep speed, in this case a sweep time of 1 s.

The YO loop assembly is another phase-locked loop. It amplifies and limits the IF output of the sampler, divides it by 10, and then corrects the YIG oscillator frequency to phase lock the IF/10 signal to a 1-MHz reference. This constrains the IF output of the sampler to be 10 MHz. The output frequency of the YIG oscillator (f_{RF}) is then:

$$f_{RF} = Nf_{LO} + 10\ \text{MHz}.$$

The harmonic number N ranges from 7 to 41. This yields a range of 2 to 20 GHz for the synthesized YIG oscillator output frequency.

This synthesis structure places stringent performance requirements on the fractional-N assembly. The frequency accuracy, resolution, and phase noise of the fractional-N loop are all multiplied by the harmonic number. Analog techniques improve the swept frequency accuracy of the phase-locked loop enough to achieve our performance goals. Excellent frequency resolution is easily attained by using 48-bit accumulators in the fractional divider. The phase noise, however, is an inherent limitation of the HP 83750 architecture because fractional-N synthesizers have higher noise than stepped synthesizers. This causes more close-in phase noise than that exhibited by traditional HP synthesizers. The fractional-N phase-locked loop bandwidth and filtering are optimized for CW phase noise. The resulting performance is better than the nonsynthesized HP 8350/83592 at almost all offsets, and the residual FM is considerably improved. This performance should easily meet the requirements of most sweeper applications.

The HP 83750 synthesizer was designed for excellent swept frequency accuracy at low cost. A fixed frequency reference replaces the high-performance stepped synthesizer used in the traditional block diagram. The digitally corrected fractional-N synthesizer is much less expensive than the fractional-N synthesizers used in previous microwave instruments. This new architecture provides synthesized frequency accuracy and broadband phase-locked sweeps at a price usually associated with open-loop sweepers.

Self-Test

The HP 83750 includes an analog bus for self-test and calibration. The analog bus is a single wire that connects to most printed circuit assemblies. Each assembly includes an analog switch that can connect the bus to any of several test points. By properly setting these switches, firmware self-test routines can measure voltages throughout the instrument using a single 12-bit analog-to-digital converter (ADC) located on the CPU board.

Over 150 tests can be executed with a single key press. When a hardware problem occurs, it can have far-reaching effects, causing a handful of test routines to report failures. For example, an incorrect power supply voltage might cause all circuits that use that voltage to "fail." Finding the most independent failure and reporting that to the operator is the goal of the diagnostic feature.

For each test in the instrument, a list of its dependencies was created. For example, the list below suggests that the test of the **Sweep Out** signal requires that the digital sweep DAC, timer #2, the timer interrupt, the DAC trigger, and the sweep trigger tests all work properly. If any of these tests has failed, then it is inappropriate to suspect the **Sweep Out** circuits as the primary cause of failure.

Test	Dependencies
SWPOUT	DIGSWPDAC
	TIMER2
	LINT_TIMER
	LDAC_TRIG
	LSWP_TRIG

After building a comprehensive table of dependencies we used a computerized algorithm to sort all tests into a single list sorted in order of interdependence. Instrument firmware uses this list to report the primary failure—the one the service technician should investigate.

Test limits can be changed in the field to accommodate hardware upgrades. A test patch feature, similar to the one used in the HP 8360 Series, allows the customer service organization to alter test limits and store them into nonvolatile memory. (The original default limits are still safely retained as well.) Self-test algorithms look for test patch limits first before using the default limits. Both default and test patch limits, as well as measured test data, can be read via the HP-IB connector (IEEE 488, IEC 625) on the rear panel.

A Digitally Corrected Fractional-N Synthesizer

Fractional dividers are used to achieve arbitrarily fine frequency resolution in a phase-locked loop synthesizer. Normally, frequency dividers can only produce integer divide ratios. Fractional division is accomplished by alternating the instantaneous divide number between N and N+1. Accumulators control the number of cycles each divide number is used. The fractional divide number is the time average of the instantaneous divide number. If a fractional divider is used in a phase-locked loop, the output frequency (f_{out}) is:

$$f_{out} = (N.F)f_{ref},$$

where N.F is the fractional divide number and f_{ref} is the phase-locked loop reference frequency.

The phase-locked loop is in fact attempting to hop the VCO frequency between Nf_{ref} and $(N+1)f_{ref}$. This causes considerable phase modulation on the VCO. Most HP fractional-N synthesizers (Fig. 1) have used a technique called analog phase interpolation (API) to remove this phase modulation.[1] API uses the accumulators that control the instantaneous divide number to predict the phase error resulting from the fractional division. A DAC sums a canceling signal into the output of the phase detector. This analog correction must be incredibly precise to achieve the necessary spurious performance.

The HP 83750 fractional-N synthesizer (Fig. 2) uses a digitally-corrected fractional divider developed at HP's Spokane Division.[2] The divider uses the same concept as sigma-delta analog-to-digital converters (ADCs). These converters operate by greatly oversampling the analog input with a coarse (often one-bit) ADC. This output is then digitally filtered to eliminate out-of-band quantization noise. Sigma-delta modulator techniques[2] can then be applied to shape the quantization noise so that most of the noise is pushed outside the frequency band of interest. The quantization noise is removed by filtering.

In the fractional divider, the fractional divide number is analogous to the analog input to the interpolative ADC. The integer divider is analogous to the one-bit ADC.

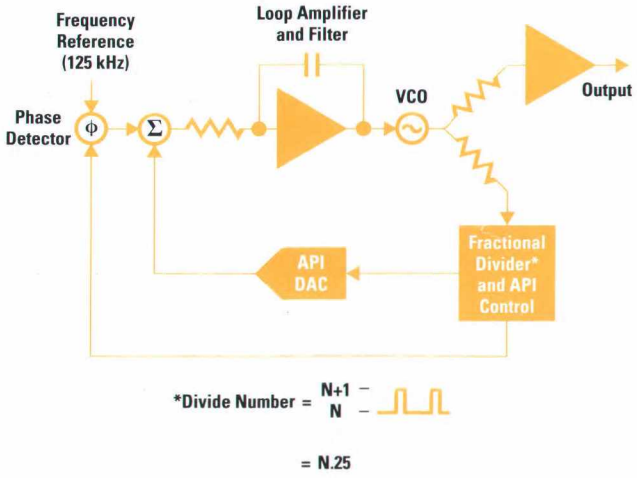

Fig. 1. The traditional fractional-N synthesizer uses an analog phase interpolator (API) to eliminate unwanted phase modulation of the VCO. The API needs 0.03% accuracy to reduce spurious sidebands to –70 dBc.

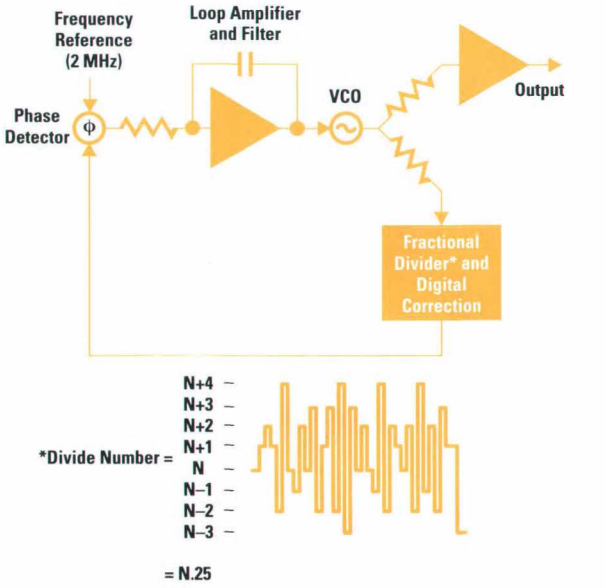

Fig. 2. The HP 83750 fractional-N synthesizer uses digital correction to shape the quantization noise. The phase-locked loop filters and removes the noise.

Digital techniques shape the fractional-division noise and push it well outside the bandwidth of the phase-locked loop. The phase-locked loop acts as a low-pass filter and removes the fractional division noise before it is applied to the VCO.

The digital correction changes the integer divide number every reference cycle, or every 500 ns in the HP 83750. The divide number is not toggled between N and N+1, but can take on any integer value between N–3 and N+4. The digital correction causes the divide number to vary in a random fashion, producing pure noise with no spurious content. This noise is shaped so that it increases at a rate of 40 dB per decade of offset frequency. The phase-locked loop low-pass filters this noise so that it never rises above the phase noise of the VCO. In this manner, the phase errors produced by fractional division are removed without the cost, size, and complexity of the API circuitry traditionally used in fractional-N synthesis.

Acknowledgments

The research and development of the fractional-N and prescaler ICs was done by Brian Miller and Bob Conley of HP's Spokane Division. They also provided consultation and support to the many users of these parts within HP.

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2. B. Miller and B. Conley, "A Multiple Modulator Fractional Divider," *Proceedings of the 44th Annual Symposium on Frequency Control*, 1990, pp. 559-568.

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A significant new feature of the HP 83750 is that instrument firmware is stored in flash EPROM, a type of reprogrammable nonvolatile memory. This allows instrument firmware to be upgraded in the field to add new features or to fix bugs. Firmware upgrades are distributed on 3.5-inch disks, which can be read using an HP 9122D HP-IB disc drive. A smaller nonreprogrammable boot ROM contains the firmware loading routine and some basic self-test routines that execute whenever the instrument is turned on.

Self-Calibration

The HP 83750 uses large arrays of calibration constants to correct for YIG filter linearity, YIG oscillator linearity, and power flatness. The instrument can generate these arrays automatically. The only other equipment required is a power meter for power calibration.

A front-panel **Peak** button causes the instrument to align the YIG filter automatically at each of approximately 230

frequencies between 2 and 20 GHz. At each frequency, the analog bus is used to monitor ALC modulator drive voltage as the YIG filter frequency is varied. When a peak is found, the proper correction value is stored in memory. This function is also called *autotracking*.

YIG oscillator calibration is available via a Special Function menu. In this case, the analog bus monitors the YO loop correction voltage and adjusts the calibration constants until the voltage is zero.

A front-panel **Flatness Cal** button allows automatic power level calibration using an HP 437B, 438A, or 70100A power meter. The user can obtain calibrated power at any point in a test system by calibrating with the power meter located at that point.

Placing time-consuming calibration routines in firmware lowers instrument cost by reducing test time. For example, autotracking via an external controller running a BASIC program took 50 minutes. The firmware autotracking routine runs in less than one minute. Faster calibration also gives better accuracy, because there is less frequency drift between the beginning and the end of the procedure.

Product Design

Ruggedness, light weight and serviceability were the goals of the HP 83750 product design. Extensive shock and vibration testing was done to ensure that the instrument meets or exceeds HP standards for ruggedness. An optional portable package with tilt-bail handle is available that meets the requirements of MIL-T-28800E Type III Class 5 Style D.

The weight was reduced through the application of modern technology. A switching power supply eliminates the heavy power transformers found in earlier designs. The dual YIG oscillator combines two separate microwave oscillators within one magnet structure. Other sweepers that use fundamental oscillators require two or three devices to cover the same frequency range, which adds to cost, weight and power consumption. An HP 83752A sweeper weighs 16 kg (35 lb) compared with 22.5 kg (49.6 lb) for an HP 8350B with HP 83592A plug-in.

Servicing an HP 83750 is facilitated by ease of access (see Fig. 8). A central cardcage houses most of the printed circuit boards. Test points are located at the top of each board. A board can also be raised on an optional extender board for more extensive troubleshooting. The power supply, bolted to the left side of the chassis, is replaceable as a unit. All microcircuits are located on an RF deck at the right side of the chassis and can be accessed by removing the top and side instrument covers. The entire RF deck can be removed from the instrument without disrupting any RF connections.

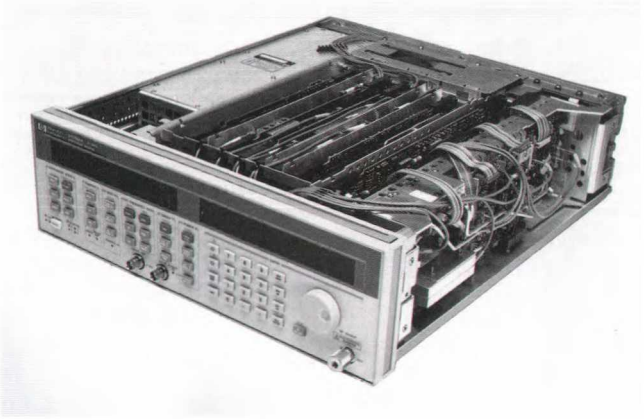

Fig. 8. Internal view of the HP 83750 chassis.

Acknowledgments

The authors would like to thank the many other engineers who made valuable technical contributions to this product. Stewart Chaimson designed the YIG driver and RF interface electronics, and developed the algorithms and data structures for YIG oscillator and filter delay compensation and linearity. Lance Haag developed calibration and alignment procedures, evaluated RF system performance, and developed the sampler assembly. Steve Punte was the technical leader and Doug Bender provided management support for firmware development. Other members of the firmware team included Jim Grishaw (hardware and HP 8757 control), Thanh Heyman (user interface), Mike Seibel (SCPI coupling and flatness calibration), Sue Wood (self-test), and Phuoc Tran and Dan Podell (firmware QA). Roger Valentine and Andy Smith did the product design. Jon Jasper was responsible for new product introduction production engineering and test development. Jon Kiser coordinated the environmental testing. We would also like to thank Arlen Dethlefsen and Rolf Dalichow for their support.

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Microcircuits for the HP 83750 Series Sweepers

Four custom microcircuits provide the basic output signal, the RF band, signal switching and distribution, amplification, ALC and pulse modulation, power amplification, and two stages of YIG filtering.

by Eric V.V. Heyman, Rick R. James, and Roger R. Graeber

This article discusses the design of the four custom microcircuits designed for the HP 83750 Series sweep oscillators. The microcircuits are:

- The dual YIG oscillator (DYO)
- The switched amplifier filter detector (SAFD)
- The 0.01-to-2-GHz heterodyne band microcircuit (HetBand)
- The combiner modulator amplifier (ModAmp).

Dual YIG Oscillator

The signal for the HP 83750 Series sweepers is generated in the dual YIG oscillator microcircuit. The DYO is actually two YIG oscillators in one magnetic housing. One oscillator covers the span from 2 to 11 GHz and the other covers from 11 to 20 GHz. The output power exceeds 20 mW from separate outputs for each band.

The high-band 11-to-20-GHz oscillator consists of a YIG resonator and a single GaAs IC chip that contains both the oscillator and buffer stages. Fig. 1 is the schematic diagram. The IC is fabricated using an HEMT GaAs IC process with an f_T of 50 GHz and an f_{max} of 100 GHz. The chip (Fig. 2) measures only 960 by 960 μm.

The oscillator stage consists of a 200-μm FET in a source follower configuration. The feedback is generated by a 0.2-pF thin-film capacitor connected between the source and ground. This feedback generates an impedance looking into the gate of the device that has a negative real part and thus has a reflection coefficient greater than 1, which is a necessary condition for oscillation to begin.[1] The condition for oscillation to begin is:

$$\Gamma_{device}\Gamma_{resonator} > 1,$$

where Γ_{device} and $\Gamma_{resonator}$ are the reflection coefficients of the device and resonator, respectively. The condition at oscillation is:

$$\Gamma_{device}\Gamma_{resonator} = 1.$$

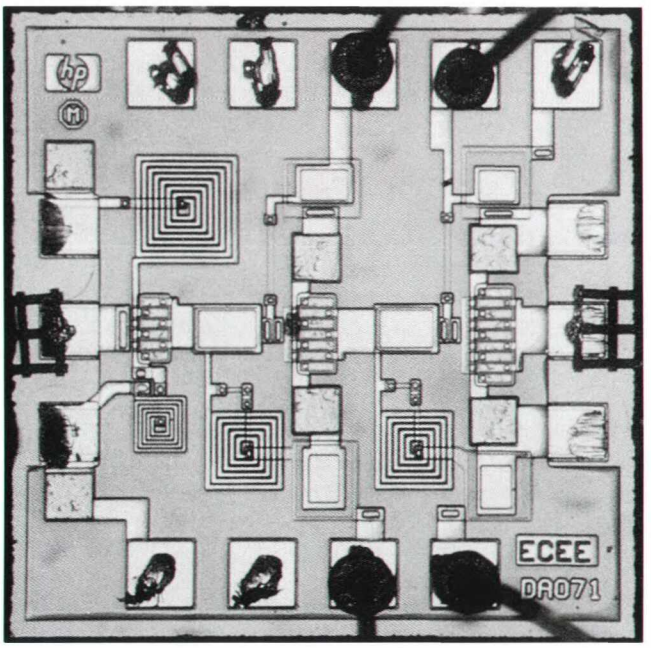

Fig. 2. Photograph of the DYO chip.

This relationship is achieved as Γ_{device} is reduced by limiting during the buildup of oscillation. The phase condition is satisfied by a shift along the resonator curve, possibly allowing the oscillation to occur somewhat off resonance.

The source follower configuration has the potential to oscillate at undesired frequencies above or below the desired band. These undesired oscillation conditions, called lockup modes, are a result of the interaction of the YIG coupling loop parasitics and the active device. The oscillator circuit must be designed so that there is insufficient reflection gain to support the lockup mode. At the low end of the band this is accomplished by placing an inductor in parallel with the

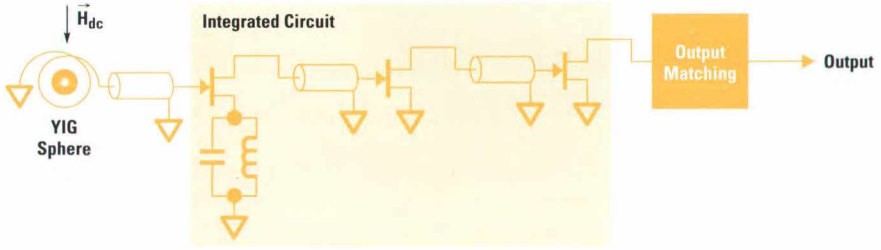

Fig. 1. DYO high-band schematic diagram.

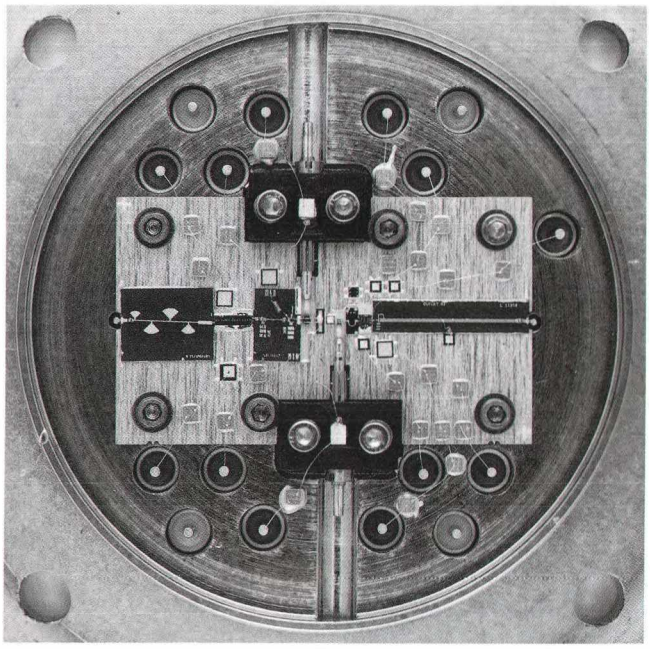

Fig. 3. Photograph of the DYO.

source feedback capacitor. This has the effect of reducing the capacitance on the source and thus the reflection gain at lower frequencies. In addition, a high-impedance coupling loop is used that does not provide the proper phase relationship for the lockup mode. To avoid lockup at the high end of the band the transmission line between the device and the resonator is kept short.

The buffer amplifier stages consist of a 300-μm FET followed by a 400-μm FET, both in the common source configuration. The oscillator stage is matched to the buffer amplifier using a short length of transmission line. The primary purpose of the buffer stages is to provide isolation and therefore a stable match to the oscillator stage, making the oscillator frequency independent of the load.

The YIG (yttrium iron garnet) resonator provides the high-Q tuning circuit for the oscillator. The high-band resonator is constructed of a 300-μm-diameter, undoped YIG sphere centered in a multiturn coupling wire. The ratio of sphere to loop diameters is a trade-off between suppression of spurious resonances and oscillation strength. The YIG resonator provides a resonance that tunes linearly with an applied magnetic field.[2]

The 11-to-20-GHz high-band oscillator is built on a 0.010-inch molybdenum carrier (Fig. 3). This carrier is held to the lid by studs inserted in the lid. The carrier's function is to provide a continuous ground plane. The YIG GaAs IC is soldered to a small heat spreader and then epoxy-attached to the carrier. A 0.010-inch fused silica microstrip circuit is epoxy-attached between the YIG resonator and the IC to provide the proper transmission line length. The output circuit is a 0.010-inch sapphire microstrip circuit which provides output matching and transition to a right-angle SMA connector.

The low-band 2-to-11-GHz oscillator consists of a YIG resonator, a bipolar transistor oscillator stage, a matching network, and a broadband buffer amplifier (Fig. 4). The oscillator stage uses a silicon bipolar transistor with an f_{max} of 22 GHz.

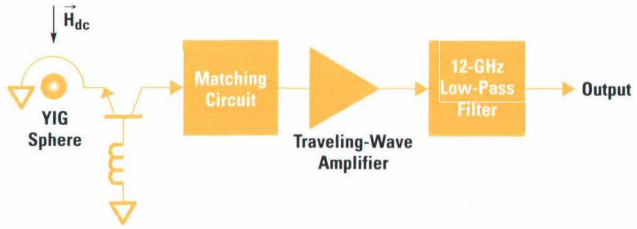

Fig. 4. DYO low-band schematic diagram.

The transistor is configured as a common base circuit with an inductor in series with the base terminal. The inductor is realized as a length of transmission line. This inductor transforms to a negative real impedance at the emitter port and thus meets the above criteria for oscillation. The collector port is terminated in a matching network that provides load conditions to optimize oscillation strength, harmonics, and linearity. The buffer stage consists of a 2-to-20-GHz traveling-wave GaAs IC amplifier. The YIG resonator consists of a 600-μm-diameter 550-gauss YIG sphere in a half loop of 950-μm-diameter wire.

The 2-to-11-GHz low-band oscillator is built on the same carrier as the high-band circuit. It uses two 0.010-inch sapphire microstrip circuits. The first circuit contains the bipolar transistor, the YIG coupling loop, and the collector matching circuit. Both the transistor and the loop are epoxy-attached to the circuit, which is also epoxy-attached to the carrier. The traveling-wave GaAs IC buffer amplifier is soldered to a heat spreader and epoxy-attached to the carrier. An output circuit provides low-pass filtering and transition to a right-angle SMA connector.

The YIG resonators require a dc magnetic field to tune the frequency. This magnetic field is applied perpendicularly to the applied RF field. The resonant frequency is related to the dc magnetic field by the equation:

$$f_o = \gamma(H_o + H_a)$$

where H_o is the applied dc magnetic field, H_a is the internal magnetic field and γ is the charge-to-mass ratio of an electron. The magnetic field is created by winding 1640 turns around a 6-mm-diameter pole tip as shown in Fig. 5. The 1.7-mm air gap under the pole tip is optimized to maximize tuning sensitivity and field uniformity, which affects the rejection of spurious resonances. The magnetic material used is a 50-50 nickel iron alloy that results in an effective magnetic saturation of over 30 GHz. The windings are wound in such a way as to optimize the internal forces when self-heating occurs. These forces can change the pole gap and therefore affect the tuning sensitivity. FM is accomplished by using a small 17-turn coil mounted on the pole tip, which adds to or subtracts from the main field.

Switched Amplifier Filter Detector

An integrated output microcircuit developed for the HP 83750 Series synthesizers provides a leveled output from 10 MHz to 20 GHz with exceptionally low harmonics and broadband noise. The goal was to create a low-cost circuit containing the required filtering, amplification, switching, and leveling in one package. Through integration, savings are realized in packaging, printed circuit boards, assembly, and testing.

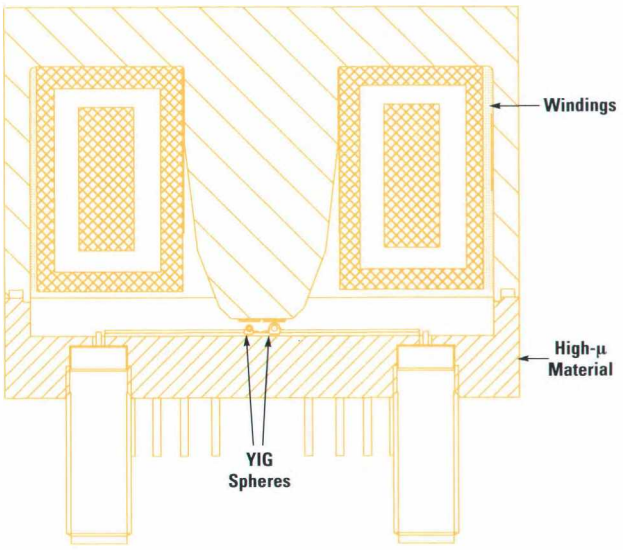

Fig. 5. Cutaway drawing of the DYO and SAFD magnet.

This microcircuit, called the switched amplifier filter detector, or SAFD, has two input paths as shown in the block diagram, Fig. 6. The low-frequency path passes 10-MHz-to-2.0-GHz signals through a thin-film low-pass filter. This filter is primarily designed to reject local oscillator feedthrough signals in the 5.4-to-7.4-GHz range. It also helps reduce harmonic signals above 3 GHz.

The high-frequency path covers 2.0 to 20 GHz. This path is designed to produce better than –45-dBc harmonics at an output power of +10 dBm. The filtering is provided by a pair of magnetically tuned YIG resonators. Since YIG filters are both lossy and exhibit power limiting characteristics, each one is carefully tuned to provide sufficient power and bandwidth. Of particular concern in this path is shielding among the various components. To attain low harmonics, it is essential to isolate each section, and in particular to isolate the YIG filters from each other. With this design, the performance is limited by the harmonics generated in the amplifier between the two resonators (without this buffer amplifier, the filters cannot be tuned independently). The amplifier is a broadband GaAs MMIC traveling-wave amplifier covering the 2-to-20-GHz range.

The magnetic field for the YIG filters is provided by two coils. A 1640-turn coil wound on a very high-permeability core provides the main 7000-gauss field within a 1.7-mm air gap to tune the YIG filters up to 20 GHz. The coil is specially designed to minimize any change in the gap size resulting from internal or external temperature variations, which would change the field intensity and thus the center frequency of the filter. It is critical that both filters are tuned to the same resonant frequency to minimize filter loss. Therefore, a small offset coil is placed close to the input filter to correct for slight differences in field strength which increase with frequency. A linear current-versus-frequency ramp is sent through this coil to compensate for the difference. Because the YIG filters must tune with the 2-to-20-GHz YIG oscillator, the packaging and magnetic design are similar to the oscillator's to reduce tracking errors.

A pair of p-i-n diodes has a dual function. Switching between the low-frequency and high-frequency paths is just a matter of turning both diodes on or off. The second function involves the bridge detector on the output. The bridge is a GaAs integrated circuit with thin-film resistors. Because of their small geometry, these resistors must be protected from dissipating excessive power. If an excessive level is detected by the bridge, clamping circuitry on the bias board shuts off the p-i-n diode bias. Under normal operation, this clamp is only a safety feature because the ALC loop in the instrument also limits the input power to the SAFD. Following the p-i-n switch, a thin-film 20-GHz low-pass filter reduces out-of-band harmonics.

The last circuit in the SAFD contains the leveling bridge. Because of proper ratioing of resistors, the voltage across the bridge diode is proportional only to the voltage incident on the load and is independent of the signal reflected from the external load. Therefore, the bridge exhibits directivity. Because the diode is operating at low power levels, its dc output voltage is proportional to the square of the voltage

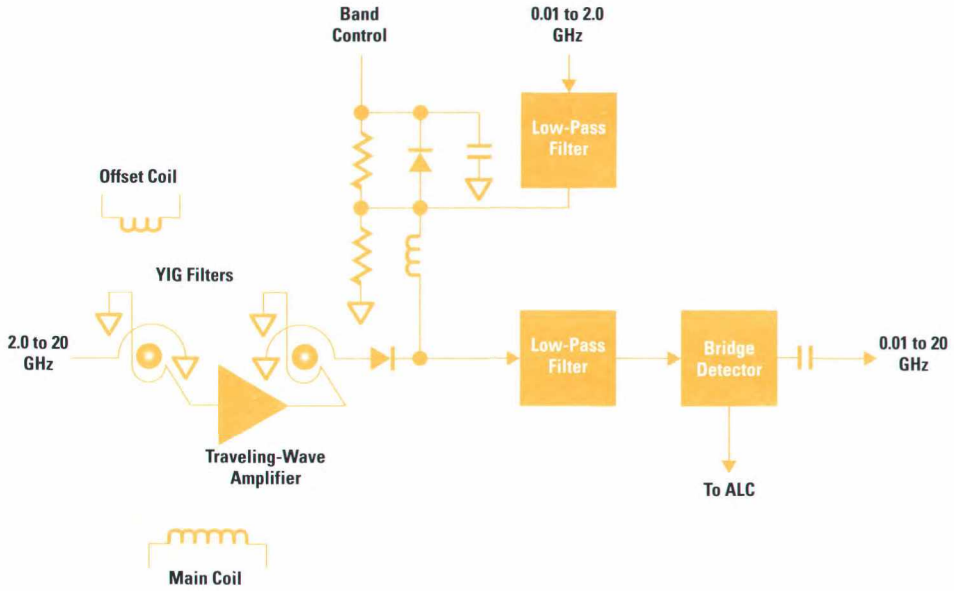

Fig. 6. SAFD microcircuit block diagram.

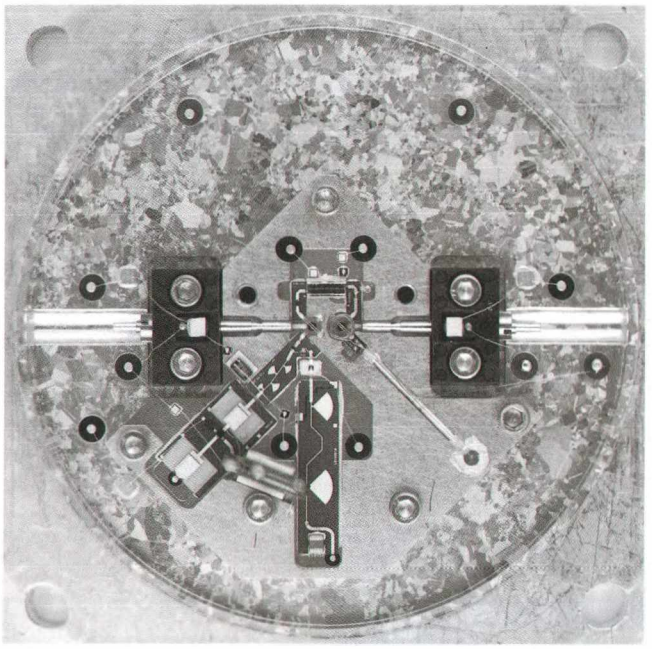

Fig. 7. SAFD microcircuit.

across it, which is proportional to the incident output power. The dc voltage from the diode is used by the ALC loop to provide improved output power flatness as a function of frequency. Because of the bridge's directivity, the leveling circuit ignores reflections from the load and thus provides a good source match.

Fig. 7 is a photograph of the SAFD microcircuit.

0.01-to-2-GHz Heterodyne Band

The 0.01-to-2-GHz band in the HP 83752A/B sweepers is generated by mixing 5.410 to 7.4 GHz (f_{LO}) from the DYO with a phase-locked 5.4-GHz (f_{RF}) oscillator in the heterodyne band microcircuit, or HetBand for short. The heart of this microcircuit is a GaAs RFIC mixer. Fig. 8 is the HetBand block diagram.

The GaAs RFIC mixer uses a doubly balanced FET bridge mixer with on-chip RF and LO phase splitting amplifiers and an on-chip differential-to-single-ended IF amplifier. Mixer design considerations include LO and RF drive levels, signal purity, and port match. Port match can be a problem at the sum and difference frequencies and at the harmonics of f_{LO} and f_{RF}. Poor port match can cause reflections back into the mixer and degrade the level of spurious signals. With a discrete mixer, performance can often be dependent on assembly techniques. The GaAs RFIC mixer has buffered RF, LO, and IF ports, making it insensitive to these assembly variations. The bias on the FET bridge mixer is the only critical adjustment. It was determined that for best performance over temperature, the mixer bias must be held to within ±0.01V of its room-temperature setting.

Measurements on the GaAs RFIC mixer indicated that there was some dependence of the 2-1 spurious product (second harmonic of f_{RF} mixing with f_{LO}) on the RF port source match at the frequency of the second harmonic, 10.8 GHz. Because it was desired to reduce the mixer's spurious products by controlling the harmonics at the RF input, there is a 6.6-GHz low-pass filter at the RF port for this purpose. As is characteristic of simple low-pass filters, the match at 10.8 GHz is very bad, since it is in the stop band. The second harmonic generated by the mixer comes out the RF port and is reflected by the poor match of the filter. The second harmonic then reenters the mixer where it is amplified and adds, in or out of phase, causing a variation in the 2-1 spurious performance. An attenuator was added to the RF input of the mixer to improve the source match and reduce the reflection back into the mixer. This reduces the 2-1 spurious product to a low enough level that a filter at the IF output can reduce the level below the spurious specification.

Amplitude modulation is done in the RF path. A broadband stagger-spaced p-i-n diode modulator is used because a quarter-wave-spaced modulator has less attenuation at the second and fourth harmonic frequencies. This ensures that there will be no increase in the harmonic levels through the modulation range, which would degrade the spurious performance.

The output power of the GaAs RFIC mixer is +5 dBm. The relatively high output power from the mixer requires less gain from the output amplifier. The lower overall gain requirement results in a low level of broadband noise. The additional power and gain are provided by a new GaAs RFIC power amplifier designed for this application. This IC is a dc coupled feedback amplifier designed specifically for high

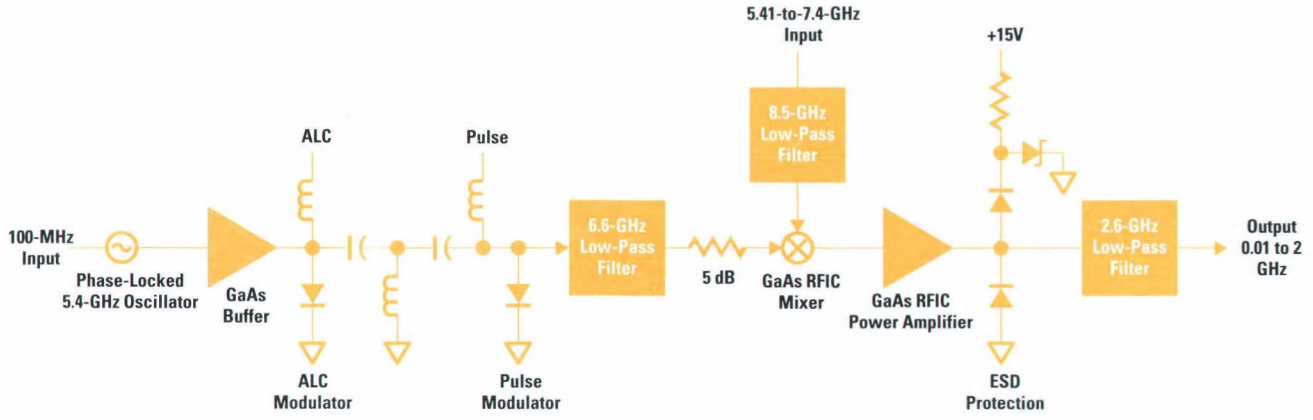

Fig. 8. HetBand microcircuit block diagram.

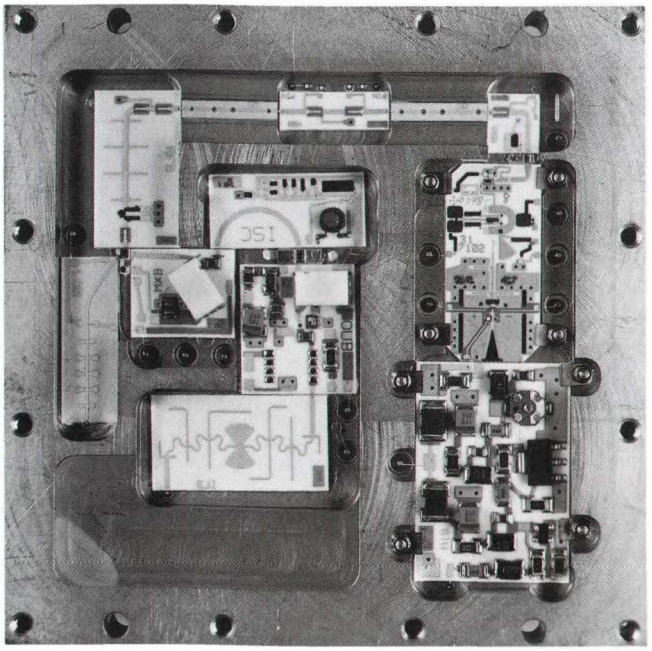

Fig. 9. HetBand microcircuit.

power, good harmonics, and wide bandwidth. ESD protection and a combination harmonic and spurious low-pass filter are added to the output.

The microcircuit is constructed in a deep-well stainless-steel package using large thick-film alumina circuits epoxy-attached directly to the package floor (Fig. 9). This eliminates the need for circuit clamps. A tellurium copper heat sink is mounted into the package floor with the RFIC power amplifier mounted directly to this heat sink. The heat sink extends out the back of the package and has fins for cooling machined into it. This combination provides the low thermal expansion of stainless steel and the high thermal conductivity of copper.

Combiner Modulator Amplifier

The ModAmp, short for combiner modulator amplifier, combines the low-band and high-band signals from the dual YIG oscillator (DYO) and redirects them to the HetBand or SAFD microcircuits. A signal is also sent to the sampler for phase locking. The ModAmp provides a pulse modulator and amplitude modulation for the ALC circuit.

The DYO has two outputs: a low band, 2 to 11 GHz, and a high band, 11 to 20 GHz. Each DYO output must be switched to the buffer amplifier and must be available at the sampler output port. In addition, the DYO low-band output must be switched to the 0.01-to-2-GHz HetBand microcircuit. The switch and coupler configuration are shown in Fig. 10, the ModAmp block diagram. The 11-to-20-GHz coupler is the load for the 2-to-11-GHz coupler. The advantage is that instead of having to design a 2-to-20-GHz coupler, we need only two simpler narrowband couplers. If a single broadband coupler were used, then there would have to be a switch at the input to combine the DYO outputs and a switch after the coupler to switch the output to the HetBand. By using two couplers, one switch is eliminated from both the heterodyne path and the 11-to-20-GHz path, thereby reducing the path loss in these two bands.

A GaAs IC buffer amplifier is placed between the reflective ALC modulator and the DYO. This buffer prevents amplitude modulation resulting from the reflective modulators from entering the sampler port and causing AM-to-PM conversion in the sampler. The pulse and AM modulators use the p-i-n diode modulators developed previously.[3] A high-pass filter between the two modulators reduces the cross talk between the modulators. Following the pulse modulator is a gain and a power stage to drive the SAFD.

The ModAmp is built in a deep-well stainless-steel package with 0.010-inch sapphire and alumina thin-film circuits epoxy-attached directly to the package floor (Fig. 11). The modulators are placed in a 3-mm channel machined into the package floor. The channels form a waveguide operating below cutoff to provide the isolation that deep modulation requires.

Acknowledgments

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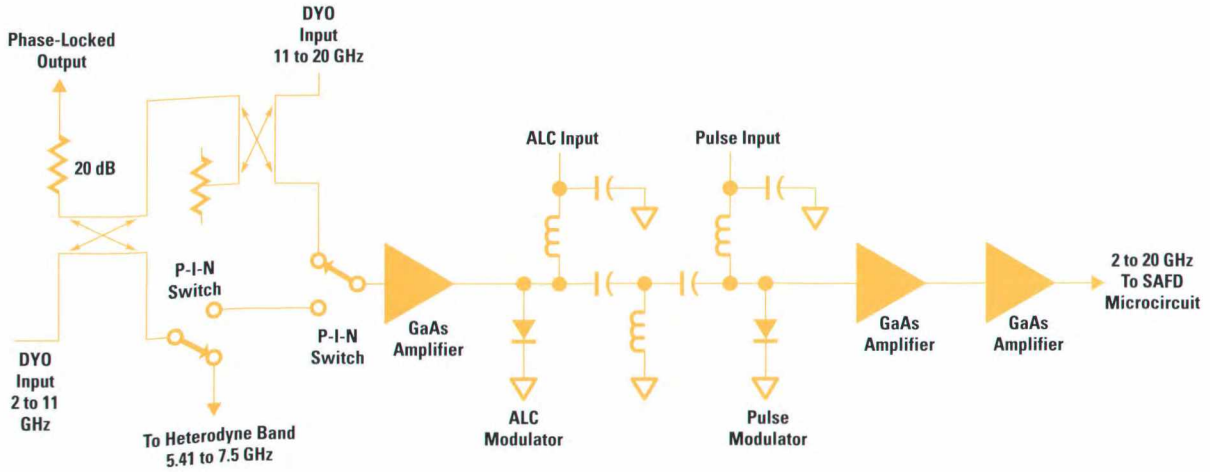

Fig. 10. ModAmp microcircuit block diagram.

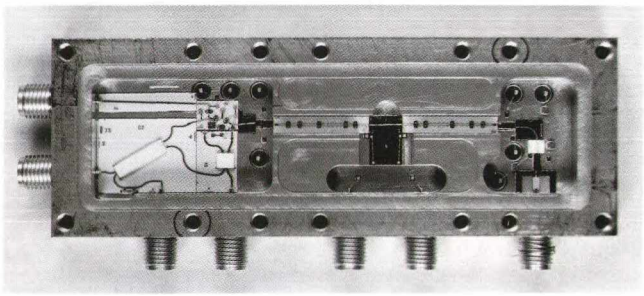

Fig. 11. ModAmp microcircuit.

oscillator development, Doug Fullmer and Julio Perdomo for their work on the high-band GaAs IC, and Mike Sohigian and Arlen Dethlefsen for their guidance.

The SAFD microcircuit was made possible by the efforts of Jim Grishaw, microwave design engineer, Andy Smith, mechanical design engineer, Eric Ehlers, ALC bridge designer, and Lance Haag, systems engineer.

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